DISPLAY DRIVER AND ELECTRO-OPTICAL DEVICE

Japanese Patent Application No. 2003-23668, filed on January 31, 2003, is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a display driver and an electro-optical device.

A display panel (display device in a broad sense) represented by a liquid crystal display (LCD) panel is mounted on portable telephones and personal digital assistants (PDAs). In particular, an LCD panel realizes reduction of the size, power consumption, and cost in comparison with other display panels, and is mounted on various electronic instruments.

An LCD panel is required to have a size equal to or greater than a certain size taking visibility of a display image into consideration. There has been a demand that the mounting size of the LCD panel be as small as possible when the LCD panel is mounted on electronic instruments.

BRIEF SUMMARY OF THE INVENTION

One aspect of the present invention relates to a display driver which drives a plurality of data lines of an electro-optical device which includes a plurality of scan lines, the data lines, a switching element connected with one of the scan lines and one of the data lines and a pixel electrode connected with the switching element, the data lines including data line groups alternately distributed from two opposite sides toward inside of the electro-optical device in a shape of comb teeth, each of the data line groups consisting of a predetermined number of the data lines, and the display driver comprising:

a gray-scale bus to which gray-scale data is supplied corresponding to an arrangement order of each of the data lines;

first and second clock lines to which a first or second shift clock is supplied;

a first shift register which includes a plurality of flip-flops, shifts a first shift start signal in a first shift direction based on the first or second shift clock on the first clock line, and outputs shift output from each of the flip-flops;

a second shift register which includes a plurality of flip-flops, shifts a second shift start signal in a second shift direction opposite to the first shift direction based on the first or second shift clock on the second clock line, and outputs shift output from each of the flip-flops;

a first data latch which includes a plurality of flip-flops, each of which holds the gray-scale data corresponding to one of the data lines based on the shift output of the first shift register;

a second data latch which includes a plurality of flip-flops, each of which holds the gray-scale data corresponding to one of the data lines based on the shift output of the second shift register;

a data line driver circuit including a plurality of data output sections, each of the data output sections driving one of the data lines based on the gray-scale data held in one of the flip-flops of the first or second data latch and being disposed corresponding to the arrangement order of the data lines, and

a clock switch circuit which outputs one of the first and second shift clocks to the first clock line and outputs the other of the first and second shift clocks to the second clock line based on a mode setting signal.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a block diagram schematically showing a configuration of an electro-optical device in an embodiment of the present invention.

FIG. 2 is a schematic diagram showing a configuration of a pixel in an embodiment of the present invention.

FIG. 3 is a block diagram schematically showing a configuration of an electro-optical device including an LCD panel which is not comb-tooth distributed.

FIG. 4 is a diagram illustrating an example of a display driver disposed along the short side of an LCD panel.

FIG. 5 is illustrative of the necessity of data scramble for driving a comb-tooth distributed LCD panel.

FIG. 6A is a schematic diagram showing a first mounting state of a display driver on an LCD panel, and FIG. 6B is a schematic diagram showing a second mounting state of a display driver on an LCD panel.

FIG. 7 is a block diagram schematically showing a configuration of a display driver in an embodiment of the present invention.

FIG. 8 is a block diagram schematically showing a configuration of a data latch shown in FIG. 7.

FIG. 9 is a circuit diagram showing a configuration example of a first shift register.

FIG. 10 is a circuit diagram showing a configuration example of a second shift register.

FIG. 11 is a configuration diagram of a shift clock generation circuit in an embodiment of the present invention.

FIG. 12 is a timing diagram showing an example of generation timing of first and second reference shift clocks by a shift clock generation circuit.

FIG. 13 is a circuit diagram showing a configuration example of a shift clock generation circuit.

FIG. 14 is a timing diagram of an example of operation of the shift clock generation circuit shown in FIG. 13.

FIG. 15 is a timing diagram showing an example of an operation of a data latch of a display driver in an embodiment of the present invention.

FIG. 16 is a timing diagram showing another example of an operation of a data latch of a display driver in an embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENT

Embodiments of the present invention are described below. Note that the embodiments described hereunder do not in any way limit the scope of the invention defined by the claims laid out herein. Note also that all of the elements described below should not be taken as essential requirements for the present invention.

As an LCD panel which allows the mounting size to be reduced, a so-called comb-tooth distributed LCD panel has been known.

In order to reduce the mounting size of the LCD panel, it is effective to reduce the interconnect region between a scan driver which drives scan lines of the LCD panel and the LCD panel or to reduce the interconnect region between a display driver which drives data lines of the LCD panel and the LCD panel.

In the case where a display driver drives data lines of a comb-tooth distributed LCD panel from opposite sides of the LCD panel, it is necessary to change the order of gray-scale data supplied corresponding to the arrangement order of the data lines in a conventional LCD panel.

Since a conventional display driver cannot change the order of gray-scale data supplied corresponding to each data line, it is necessary to add a dedicated data scramble IC in the case of driving the comb-tooth distributed LCD panel by using a conventional display driver.

In the comb-tooth distributed LCD panel in which the order of gray-scale data must be changed as described above, the method of changing the order differs depending on the mounting state of the display driver.

According to the following embodiments, a display driver and an electro-optical device capable of driving a display panel in which data lines are comb-tooth distributed

corresponding to the mounting state can be provided.

The embodiments of the present invention are described below in detail with reference to the drawings.

1. Electro-optical device

FIG. 1 shows an outline of a configuration of an electro-optical device in this embodiment. FIG. 1 shows a liquid crystal device as an example of an electro-optical device. A liquid crystal device may be incorporated in various electronic instruments such as a portable telephone, portable information instrument (PDA, etc.), digital camera, projector, portable audio player, mass storage device, video camera, electronic notebook, or global positioning system (GPS).

A liquid crystal device 10 includes an LCD panel (display panel in a broad sense; electro-optical device in a broader sense) 20, a display driver (source driver) 30, and scan drivers (gate drivers) 40 and 42.

The liquid crystal device 10 does not necessarily include all of these circuit blocks. The liquid crystal device 10 may have a configuration in which some of these circuit blocks are omitted.

The liquid crystal panel 20 includes a plurality of scan lines (gate lines), a plurality of data lines (source lines) which intersect the scan lines, and a plurality of pixels, each of the pixels being specified by one of the scan lines and one of the data lines. In the case where one pixel consists of three color components of RGB, one pixel consists of three dots, one dot each for red, green and blue. The dot may be referred to as an element point which makes up each pixel. The data lines corresponding to one pixel may be referred to as data lines of the number of color components which make up one pixel. The following description is given on the assumption that one pixel consists of one dot for convenience of description.

Each of the pixels includes a thin film transistor (hereinafter abbreviated as

"TFT") (switching element) and a pixel electrode. The TFT is connected with the data line, and the pixel electrode is connected with the TFT.

The LCD panel 20 is formed on a panel substrate formed of a glass substrates, for example. A plurality of scan lines arranged in the X direction shown in FIG. 1 and extending in the Y direction, and a plurality of data lines arranged in the Y direction and extending in the X direction, are disposed on the panel substrate. In the LCD panel 20, each of the data lines is comb-tooth distributed. In FIG. 1, each of the data lines is comb-tooth distributed so as to be driven from a first side of the LCD panel 20 and a second side which faces the first side. The comb-tooth distribution may be referred to as distribution in which a given number of data lines (one or a plurality of data lines) are alternately distributed from each side (first and second sides of the LCD panel 20) toward the inside in the shape of comb teeth.

FIG. 2 schematically shows a configuration of the pixel. In FIG. 2, one pixel consists of one dot. A pixel PEmn is disposed at a location corresponding to the intersecting point of the scan line GLm ($1 \leq m \leq M$, M and m are integers) and the data line DLn ($1 \leq n \leq N$, N and n are integers). The pixel PEmn includes the TFTmn and the pixel electrode PELmn.

A gate electrode of the TFTmn is connected with the scan line GLm. A source electrode of the TFTmn is connected with the data line DLn. A drain electrode of the TFTmn is connected with the pixel electrode PELmn. A liquid crystal capacitor CLmn is formed between the pixel electrode and a common electrode COM which faces the pixel electrode through a liquid crystal element (electro-optical material in a broad sense). A storage capacitor may be formed in parallel with the liquid crystal capacitor CLmn. Transmissivity of the pixel changes corresponding to the voltage applied between the pixel electrode and the common electrode COM. A voltage VCOM supplied to the common electrode COM is generated by a power supply circuit (not shown).

The LCD panel 20 is formed by attaching a first substrate on which the pixel

electrode and the TFT are formed to a second substrate on which the common electrode is formed, and sealing a liquid crystal as an electro-optical material between the two substrates.

The scan line is scanned by the scan drivers 40 and 42. In FIG. 1, one scan line is driven by the scan drivers 40 and 42 at the same time.

The data line is driven by the display driver 30. The data line is driven by the display driver 30 from the first side of the LCD panel 20 or the second side of the LCD panel 20 which faces the first side. The first and second sides of the LCD panel 20 face in the direction in which the data lines extend.

In the LCD panel 20 in which the data lines are comb-tooth distributed, the data lines are comb-tooth distributed so that the data lines of the number of color components of each pixel disposed corresponding to the adjacent pixels connected with the selected scan line are driven from opposite directions.

In more detail, in the LCD panel 20 in which the data lines are comb-tooth distributed shown in FIG. 2, in the case where the data lines DLn and DL(n + 1) are disposed corresponding to the adjacent pixels connected with the selected scan line GLm, the data line DLn is driven by the display driver 30 from the first side of the LCD panel 20, and the data line DL(n + 1) is driven by the display driver 30 from the second side of the LCD panel 20.

This also applies to the case where the data lines corresponding to each color component of RGB are disposed corresponding to one pixel. In this case, if the data line DLn consisting of a set of three color component data lines (Rn, Gn, Bn) and the data line DL(n + 1) consisting of a set of three color component data lines (R(n + 1), G(n + 1), B(n + 1)) are disposed corresponding to the adjacent pixels connected with the selected scan line GLm, the data line DLn is driven by the display driver 30 from the first side of the LCD panel 20, and the data line DL(n + 1) is driven by the display driver 30 from the second side of the LCD panel 20.

The display driver 30 drives the data lines DL1 to DLN of the LCD panel 20 based on gray-scale data for one horizontal scanning period supplied in units of horizontal scanning periods. In more detail, the display driver 30 drives at least one of the data lines DL1 to DLN based on the gray-scale data.

The scan drivers 40 and 42 drives the scan lines GL1 to GLM of the LCD panel 20. In more detail, the scan drivers 40 and 42 consecutively select the scan lines GL1 to GLM in one vertical period, and drive the selected scan line.

The display driver 30 and the scan drivers 40 and 42 are controlled by a controller (not shown). The controller outputs control signals to the display driver 30, the scan drivers 40 and 42, and the power supply circuit according to the contents set by a host such as a central processing unit (CPU). In more detail, the controller supplies an operation mode setting and a horizontal synchronization signal or a vertical synchronization signal generated therein to the display driver 30 and the scan drivers 40 and 42, for example. The horizontal synchronization signal specifies the horizontal scanning period. The vertical synchronization signal specifies the vertical scanning period. The controller controls the power supply circuit relating to polarity reversal timing of the voltage VCOM applied to the common electrode COM.

The power supply circuit generates various voltages applied to the LCD panel 20 and the voltage VCOM applied to the common electrode COM based on a reference voltage supplied from the outside.

In FIG. 1, the liquid crystal device 10 may include the controller, or the controller may be provided outside the liquid crystal device 10. The host (not shown) may be included in the liquid crystal device 10 together with the controller.

At least one of the scan drivers 40 and 42, the controller, and the power supply circuit may be included in the display driver 30.

Some or all of the display driver 30, the scan drivers 40 and 42, the controller, and the power supply circuit may be formed on the LCD panel 20. For example, the display

driver 30 and the scan drivers 40 and 42 may be formed on the LCD panel 20. In this case, the LCD panel 20 may also be called an electro-optical device. The LCD panel 20 may be formed to include the data lines, the scan lines, the pixels, each of which is specified by one of the data lines and one of the scan lines, the display driver which drives the data lines, and the scan driver which scans the scan line. The pixels are formed in a pixel formation region of the LCD panel 20.

The advantages of the comb-tooth distributed LCD panel is described below.

FIG. 3 schematically shows a configuration of an electro-optical device including an LCD panel which is not comb-tooth distributed. An electro-optical device 80 shown in FIG. 3 includes an LCD panel 90 which is not comb-tooth distributed. In the LCD panel 90, each of the data lines is driven by a display driver 92 from a first side. Therefore, an interconnect region for connecting each of data output sections of the display driver 92 with each of the data lines of the LCD panel 90 is necessary. If the number of data lines is increased and the lengths of the first and second sides of the LCD panel 90 are increased, it is necessary to bend each interconnect, whereby the width W0 for the interconnect region is necessary.

On the contrary, in the electro-optical device 10 shown in FIG. 1, only the widths W1 and W2 which are smaller than the width W0 are necessary on the first and second sides of the LCD panel 20.

Taking mounting on electronic instruments into consideration, an increase in the length of the LCD panel (electro-optical device) in the direction of the short side is inconvenient in comparison with the case where the length of the LCD panel is increased in the direction of the long side to some extent. This is not desirable from the viewpoint of the design, since the frame of the display section of the electronic instrument is increased, for example.

In FIG. 3, the length of the LCD panel is increased in the direction of the short side. In FIG. 1, the length of the LCD panel is increased in the direction of the long side.

Therefore, the widths of the interconnect regions on the first and second sides can be made narrow to almost an equal extent. In FIG. 1, the area of the non-interconnect region in FIG. 3 can be reduced, whereby the mounting size can be reduced.

In the case where the arrangement order of the data output sections of the display driver 30 corresponds to the arrangement order of data lines of the LCD panel 20, the interconnects which connect the data output sections with the data lines can be disposed from the first and second sides by disposing the display driver 30 along the short side of the LCD panel 20 as shown in FIG. 4, whereby the interconnects can be simplified and the interconnect region can be reduced.

However, in the case of driving the LCD panel 20, in the display driver 30 which receives gray-scale data output by a general-purpose controller corresponding to the arrangement order of the data lines, it is necessary to change the order of the received gray-scale data.

The following description is given on the assumption that the display driver 30 includes data output sections OUT1 to OUT320, and the data output sections are arranged in the direction from the first side to the second side. Each of the data output sections corresponds to each of the data lines of the LCD panel 20.

A general-purpose controller supplies gray-scale data DATA1 to DATA320 respectively corresponding to the data lines DL1 to DL320 to the display driver 30 in synchronization with a reference clock CPH as shown in FIG. 5. In the case where the display driver 30 drives the LCD panel which is not comb-tooth distributed as shown in FIG. 3, since the data output section OUT1 is connected with the data line DL1, the data output section OUT2 is connected with the data line DL2, ..., and the data output section OUT320 is connected with the data line DL320, an image can be displayed without causing a problem. However, in the case where the display driver 30 drives the comb-tooth distributed LCD panel as shown in FIG. 1 or 4, since the data output section OUT1 is connected with the data line DL1, the data output section OUT2 is connected

with the data line DL3, ..., and the data output section OUT320 is connected with the data line DL2, a desired image cannot be displayed.

Therefore, it is necessary to change the arrangement of the gray-scale data as shown in FIG. 5 by performing scramble processing which changes the order of the gray-scale data. Therefore, in the case of driving the comb-tooth distributed LCD panel by using a display driver controlled by a general-purpose controller, a dedicated data scramble IC which performs the above scramble processing is added, whereby the mounting size is inevitably increased.

The display driver 30 in this embodiment is capable of driving the comb-tooth distributed LCD panel based on the gray-scale data supplied from a general-purpose controller by the configuration described below.

In the case of driving the data lines of the comb-tooth distributed LCD panel 20 by using the display driver 30, it is necessary to change the arrangement order of the gray-scale data corresponding to the mounting state of the display driver 30.

FIG. 6A schematically shows a first mounting state of the display driver 30 with respect to the LCD panel 20. FIG. 6B schematically shows a second mounting state of the display driver 30 with respect to the LCD panel 20.

In this example, the display driver 30 is capable of changing the arrangement order of the gray-scale data in order to display an image shown in FIG. 6A. Therefore, the display driver 30 captures the gray-scale data DATA1, DATA2, DATA3, ... in the order of the data output section OUT1, the data output section OUT320, and the data output section OUT3, ... as shown in FIG. 5 (first mounting state).

However, in the case where the display driver 30 captures the gray-scale data in the same order in the second mounting state, since the drive voltage based on the gray-scale data DATA1 is output from the data output section OUT1, the image shown in FIG. 6B cannot be displayed.

A problem same as above also happens when mounting the display driver 30 to

the LCD panel 20 since a facing surface of a chip of the display driver 30 to the LCD panel 20 is determined, such as facing the front surface or back surface of the chip to the LCD panel 20.

As described above, the arrangement order of the gray-scale data and the capture start order of the gray-scale data must be changed corresponding to the mounting state of the display driver 30.

2. Display driver

FIG. 7 shows an outline of a configuration of the display driver 30. The display driver 30 includes a data latch 100, a line latch 200, a digital-to-analog converter (DAC) (voltage select circuit in a broad sense) 300, and a data line driver circuit 400.

The data latch 100 captures gray-scale data in one horizontal scanning cycle.

The line latch 200 latches the gray-scale data captured by the data latch 100 based on the horizontal synchronization signal Hsync.

The DAC 300 selectively outputs the drive voltage (gray-scale voltage) corresponding to the gray-scale data from the line latch 200 in units of data lines from a plurality of reference voltages, each of which corresponds to the gray-scale data. In more detail, the DAC 300 decodes the gray-scale data from the line latch 200, and selects one of the reference voltages based on the decode result. The reference voltage selected by the DAC 300 is output to the data line driver circuit 400 as the drive voltage.

The data line driver circuit 400 includes 320 data output sections OUT1 to OUT320. The data line driver circuit 400 drives the data lines DL to DLN based on the drive voltage from the DAC 300 through the data output sections OUT1 to OUT320. In the data line driver circuit 400, the data output sections (OUT1 to OUT320), each of which drives each of the data lines based on the gray-scale data (latch data) held in the line latch 200 (first or second flip-flop of the data latch), are disposed corresponding to the arrangement order of the data lines. The above description illustrates the case where

the data line driver circuit 400 includes the 320 data output sections OUT1 to OUT320. However, the number of data output sections is not limited.

In the display driver 30, latch data LAT1 captured by the data latch 100 is output to the line latch 200. The latch data LLAT1 latched by the line latch 200 is output to the DAC 300. The DAC 300 generates a drive voltage GV1 corresponding to the latch data LLAT1 from the line latch 200. The data output section OUT1 of the data line driver circuit 400 drives the data line connected with the data output section OUT1 based on the drive voltage GV1 from the DAC 300.

As described above, the display driver 30 captures the gray-scale data into the data latch 100 in units of data output sections of the data line driver circuit 400. The latch data latched by the data latch 100 in units of the data output sections may be in units of one pixel, a plurality of pixels, one dot, or a plurality of dots.

FIG. 8 shows an outline of a configuration of the data latch 100 shown in FIG. 7. The data latch 100 includes a gray-scale bus 110, first and second clock lines 120 and 130, first and second shift registers 140 and 150, first and second data latches 160 and 170, and a clock switch circuit 180.

The gray-scale data is supplied to the gray-scale bus 110 corresponding to the arrangement order of the data lines DL1 to DLN. A first shift clock CLK1 is supplied to the first clock line 120. A second shift clock CLK2 is supplied to the second clock line 130.

The first shift register 140 includes a plurality of flip-flops. The first shift register 140 shifts a first shift start signal ST1 in a first shift direction based on the first shift clock CLK1, and outputs shift outputs from each flip-flop. The first shift direction may be the direction from the first side to the second side of the LCD panel 20. Shift outputs SFO1 to SFO160 of the first shift register 140 are output to the first data latch 160.

FIG. 9 shows a configuration example of the first shift register 140. In the first shift register 140, D flip-flops (hereinafter abbreviated as "DFF") DFF1 to DFF160 are

connected in series so that the first shift start signal ST1 is shifted in the first shift direction. A Q terminal of the DFFk ($1 \leq k \leq 159$, k is a natural number) is connected with a D terminal of the DFF(k + 1) in the subsequent stage. Each of the DFFs captures and holds the signal input to the D terminal at a rising edge of the signal input to a C terminal, and outputs the held signal from the Q terminal as the shift output SFO.

In FIG. 8, the second shift register 150 includes a plurality of flip-flops. The second shift register 150 shifts a second shift start signal ST2 in a second shift direction opposite to the first direction based on the second shift clock CLK2, and outputs shift outputs from each flip-flop. The second shift direction may be the direction from the second side to the first side of the LCD panel 20. Shift outputs SFO161 to SFO320 of the second shift register 150 are output to the second data latch 170.

FIG. 10 shows a configuration example of the second shift register 150. In the second shift register 150, DFF320 to DFF161 are connected in series so that the second shift start signal ST2 is shifted in the second shift direction. A Q terminal of the DFFj ($162 \leq j \leq 320$, j is a natural number) is connected with a D terminal of the DFF(j-1) in the subsequent stage. Each of the DFFs captures and holds the signal input to the D terminal at a rising edge of the signal input to a C terminal, and outputs the held signal from the Q terminal as the shift output SFO.

In FIG. 8, the first data latch 160 includes a plurality of flip-flops (FF) 1 to 160 (not shown), each of which corresponds to one of the data output sections OUT1 to OUT160. The FFi ($1 \leq i \leq 160$) holds the gray-scale data on the gray-scale bus 110 based on the shift output SFOi of the first shift register 140. The gray-scale data held in the flip-flops of the first data latch 160 is output to the line latch 200 as the latch data LAT1 to LAT160.

The second data latch 170 includes a plurality of flip-flops (FF) 161 to 320 (not shown), each of which corresponds to one of the data output sections OUT161 to OUT320. The FFi ($161 \leq i \leq 320$) holds the gray-scale data on the gray-scale bus 110

based on the shift output SFOi of the second shift register 150. The gray-scale data held in the flip-flops of the second data latch 170 is output to the line latch 200 as the latch data LAT161 to LAT320.

As described above, the first and second data latches 160 and 170 are capable of capturing the gray-scale data on the gray-scale bus 110 connected in common based on the shift outputs which can be separately generated. This enables the latch data corresponding to each of the data output sections to be captured into the data latch 100 by changing the arrangement order of the gray-scale data on the gray-scale bus. Therefore, the comb-tooth distributed LCD panel 20 can be driven without using a data scramble IC by driving the data lines from the first side of the LCD panel 20 (electro-optical device) based on the data (LAT1 to LAT160) held in the flip-flops of the first data latch 160 and driving the data lines from the second side of the LCD panel 20 (electro-optical device) based on the data (LAT161 to LAT320) held in the flip-flops of the second data latch 170.

In FIG. 8, the clock switch circuit 180 outputs one of the first and second shift clocks CLK1 and CLK2 to the first clock line 120 and outputs the other of the first and second shift clocks CLK1 and CLK2 to the second clock line 130 based on a given mode setting signal. The mode setting signal is a signal set corresponding to the mounting state of the display driver 30.

In more detail, the clock switch circuit 180 outputs a first reference shift clock CLK10 to the first clock line 120 as the first shift clock CLK1 and outputs a second reference shift clock CLK20 to the second clock line 130 as the second shift clock CLK2 when the mode setting signal is "H" (first level). The clock switch circuit 180 outputs the second reference shift clock CLK20 to the first clock line 120 as the first shift clock CLK1 and outputs the first reference shift clock CLK10 to the second clock line 130 as the second shift clock CLK2 when the mode setting signal is "L" (second level).

In this embodiment, since the shift clocks output to the first and second clock lines 120 and 130 can be replaced by using the mode setting signal, the capture start order of

the gray-scale data by the first and second shift registers 140 and 150 can be changed. Therefore, the arrangement order of the gray-scale data and the capture start order of the gray-scale data can be changed corresponding to the mounting state of the display driver 30.

It is preferable that the display driver 30 include the following shift clock generation circuit.

FIG. 10 shows an outline of a configuration of a shift clock generation circuit. A shift clock generation circuit 500 generates the first and second reference shift clocks CLK10 and CLK20 based on a reference clock CPH with which the gray-scale data is supplied in synchronization. The shift clock generation circuit 500 generates the first and second reference shift clocks CLK10 and CLK20 so as to include a period in which the phases of the first and second reference shift clocks CLK10 and CLK20 are reversed. This enables the first and second shift clocks CLK1 and CLK2 for obtaining the shift outputs generated separately to be generated by using a simple configuration.

In the shift clock generation circuit 500, the first and second shift start signals ST1 and ST2 may be signals having the same phase by generating the first and second shift clocks CLK1 and CLK2 by using the first and second reference shift clocks CLK10 and CLK20 as described below, whereby the configuration and control can be simplified.

FIG. 12 shows an example of generation timing of the first and second reference shift clocks CLK10 and CLK20 by the shift clock generation circuit 500. In order to allow the first and second shift start signals ST1 and ST2 to be signals having the same phase, it is necessary to capture the first and second shift start signals ST1 and ST2 in the first-stages of the first and second shift registers 140 and 150, respectively.

Therefore, the shift clock generation circuit 500 generates a clock select signal CLK_SELECT which specifies a first-stage capture period and a data capture period (shift operation period). The first-stage capture period may be referred to as a period in which the first shift start signal ST1 is captured into the first shift register 140, or a period

in which the second shift start signal ST2 is captured into the second shift register 150. The data capture period may be referred to as a period in which the shift start signals captured in the first-stage capture period are shifted after the first-stage capture period has elapsed.

The first and second reference shift clocks CLK10 and CLK20 are provided with edges for capturing the first and second shift start signals ST1 and ST2 by using the clock select signal CLK_SELECT.

Therefore, a pulse P1 of the reference clock CPH is generated in the first-stage capture period. A frequency-divided clock CPH2 is generated by dividing the frequency of the reference clock CPH. The frequency-divided clock CPH2 becomes the second reference shift clock CLK20. An inverted frequency-divided clock XCPH2 is generated by reversing the phase of the frequency-divided clock CPH2.

The first reference shift clock CLK10 is generated by selectively outputting the pulse P1 of the reference clock CPH in the first-stage capture period and selectively outputting the inverted frequency-divided clock XCPH2 in the data capture period by using the clock select signal CLK_SELECT.

The first and second reference shift clocks CLK10 and CLK20 generated in this manner are switched corresponding to the mode setting signal and output as the first and second shift clocks CLK1 and CLK2.

FIG. 13 shows a circuit diagram which is a specific configuration example of the shift clock generation circuit 500.

FIG. 14 shows an example of operation timing of the shift clock generation circuit 500 shown in FIG. 13.

In FIGS. 13 and 14, clocks CLK_A and CLK_B are generated by using the reference clock CPH and selectively output by the clock select signal CLK_SELECT. The second reference shift clock CLK20 is a signal obtained by reversing the clock CLK_B. The first reference shift clock CLK10 is the clock CLK_A selectively output in

the first-stage capture period in which the clock select signal CLK_SELECT is "L", and the clock CLK_B selectively output in the data capture period in which the clock select signal CLK_SELECT is "H".

The operation of the data latch 100 of the display driver 30 having the above-described configuration is described below.

FIG. 15 shows an example of an operation timing chart of the data latch 100 of the display driver 30.

FIG. 15 shows a timing example in the case where the mode setting signal is set at "H". The first and second reference shift clocks CLK10 and CLK20 are generated as shown in FIGS. 12 and 14, and the first and second shift start signals ST1 and ST2 are signals having the same phase.

The gray-scale data is supplied to the gray-scale bus 110 corresponding to the arrangement order of the data lines DL1 to DLN of the LCD panel 20. In this example, the gray-scale data DATA1 ("1" in FIG. 15) is illustrated corresponding to the data line DL1 and the gray-scale data DATA2 ("2" in FIG. 15) is illustrated corresponding to the data line DL2.

The first shift register 140 shifts the first shift start signal ST1 in synchronization with the rising edge of the first shift clock CLK1. As a result, the first shift register 140 outputs the shift outputs SFO1 to SFO160 in that order.

The second shift register 150 shifts the second shift start signal ST2 in synchronization with the rising edge of the second shift clock CLK2 during the shift operation of the first shift register 140. As a result, the second shift register 150 outputs the shift outputs SFO320 to SFO161 in that order.

The first data latch 160 captures the gray-scale data on the gray-scale bus 110 at the falling edge of each shift output from the first shift register 140. As a result, the first data latch 160 captures the gray-scale data DATA1 at the falling edge of the shift output SFO1, captures the gray-scale data DATA3 at the falling edge of the shift output SFO2,

and captures the gray-scale data DATA5 at the falling edge of the shift output SFO3.

The second data latch 170 captures the gray-scale data on the gray-scale bus 110 at the falling edge of each shift output from the second shift register 150. As a result, the second data latch 170 captures the gray-scale data DATA2 at the falling edge of the shift output SFO320, captures the gray-scale data DATA4 at the falling edge of the shift output SFO319, and captures the gray-scale data DATA6 at the falling edge of the shift output SFO318.

This enables the gray-scale data after the data scramble (see FIG. 5) corresponding to each of the data lines of the comb-tooth distributed LCD panel 20 to be captured. Therefore, the gray-scale data DATA1 to DATA320 is respectively supplied to each of the data lines DL1 to DL320 of the LCD panel 20 shown in FIG. 1 or 4, whereby a correct image can be displayed.

FIG. 16 shows another example of the operation timing chart of the data latch 100 of the display driver 30.

FIG. 16 shows a timing example in the case where the mode setting signal is set at "L". Therefore, the first and second shift clocks CLK1 and CLK2 are replaced in comparison with FIG. 15. The first and second reference shift clocks CLK10 and CLK20 are generated as shown in FIGS. 12 and 14, and the first and second shift start signals ST1 and ST2 are signals having the same phase.

The first shift register 140 shifts the first shift start signal ST1 in synchronization with the rising edge of the first shift clock CLK1. As a result, the first shift register 140 outputs the shift outputs SFO1 to SFO160 in that order.

The second shift register 150 shifts the second shift start signal ST2 in synchronization with the rising edge of the second shift clock CLK2 during the shift operation of the first shift register 140. As a result, the second shift register 150 outputs the shift outputs SFO320 to SFO161 in that order.

The first data latch 160 captures the gray-scale data on the gray-scale bus 110 at

the falling edge of each shift output from the first shift register 140. As a result, the first data latch 160 captures the gray-scale data DATA2 at the falling edge of the shift output SFO1, captures the gray-scale data DATA4 at the falling edge of the shift output SFO2, and captures the gray-scale data DATA6 at the falling edge of the shift output SFO3.

The second data latch 170 captures the gray-scale data on the gray-scale bus 110 at the falling edge of each shift output from the second shift register 150. As a result, the second data latch 170 captures the gray-scale data DATA1 at the falling edge of the shift output SFO320, captures the gray-scale data DATA3 at the falling edge of the shift output SFO319, and captures the gray-scale data DATA5 at the falling edge of the shift output SFO318.

This enables drive based on the gray-scale data DATA1 from the data output section OUT320 and drive based on the gray-scale data DATA2 from the data output section OUT1 as shown in FIG. 6B to be performed by changing the capture start timing of the gray-scale data, whereby a correct image can be displayed even in the case shown in FIG. 6B.

The present invention is not limited to the above-described embodiment. Various modifications and variations are possible within the spirit and scope of the present invention. The above embodiment is described taking as an example an active matrix type liquid crystal panel in which each pixel of the display panel includes a TFT. However, the present invention is not limited thereto. The present invention can also be applied to a passive matrix type liquid crystal display. The present invention can be applied to a plasma display device in addition to the liquid crystal panel.

In the case of forming one pixel by using three dots, the present invention can be realized in the same manner as described above by replacing the data line by a set of three color component data lines.

Part of requirements of any claim of the present invention could be omitted from a dependent claim which depends on that claim. Moreover, part of requirements of any

independent claim of the present invention could be made to depend on any other independent claim.

The following items are disclosed relating to the above-described embodiment.

One embodiment of the present invention provides a display driver which drives a plurality of data lines of an electro-optical device which includes a plurality of scan lines, the data lines, a switching element connected with one of the scan lines and one of the data lines and a pixel electrode connected with the switching element, the data lines including data line groups alternately distributed from two opposite sides toward inside of the electro-optical device in a shape of comb teeth, each of the data line groups consisting of a predetermined number of the data lines, and the display driver including:

a gray-scale bus to which gray-scale data is supplied corresponding to an arrangement order of each of the data lines;

first and second clock lines to which a first or second shift clock is supplied;

a first shift register which includes a plurality of flip-flops, shifts a first shift start signal in a first shift direction based on the first or second shift clock on the first clock line, and outputs shift output from each of the flip-flops;

a second shift register which includes a plurality of flip-flops, shifts a second shift start signal in a second shift direction opposite to the first shift direction based on the first or second shift clock on the second clock line, and outputs shift output from each of the flip-flops;

a first data latch which includes a plurality of flip-flops, each of which holds the gray-scale data corresponding to one of the data lines based on the shift output of the first shift register;

a second data latch which includes a plurality of flip-flops, each of which holds the gray-scale data corresponding to one of the data lines based on the shift output of the second shift register;

a data line driver circuit including a plurality of data output sections, each of the

data output sections driving one of the data lines based on the gray-scale data held in one of the flip-flops of the first or second data latch and being disposed corresponding to the arrangement order of the data lines, and

a clock switch circuit which outputs one of the first and second shift clocks to the first clock line and outputs the other of the first and second shift clocks to the second clock line based on a mode setting signal.

In this embodiment, the gray-scale data supplied to the gray-scale bus corresponding to the arrangement order of each of the data lines of the electro-optical device can be captured into the first and second data latches by the shift outputs based on the first and second shift clocks which can be separately set. The first and second shift clocks can be selectively output to the first and second clock lines corresponding to the mode setting signal by the clock switch circuit.

This enables the gray-scale data to be captured into the first and second data latches by changing the arrangement order of the gray-scale data on the gray-scale bus. Therefore, a comb-tooth distributed electro-optical device can be driven without using a data scramble IC as an additional circuit. Moreover, the capture start order of the gray-scale data by the first and second shift registers can be changed by outputting the first and second shift clocks while replacing the first and second shift clocks.

With this display driver, the data line driver circuit may drive the data lines from a first side of the electro-optical device based on data held in the flip-flops of the first data latch, and may drive the data lines from a second side of the electro-optical device which faces the first side based on data held in the flip-flops of the second data latch.

According to this feature, the mounting size of the comb-tooth distributed electro-optical device can be reduced by driving the data lines from the first side based on the data held in the flip-flops of the first data latch, and driving the data lines from the second side of the electro-optical device which faces the first side based on the data held in the flip-flops of the second data latch.

With this display driver, the clock switch circuit may output a first reference shift clock to the first clock line as the first shift clock and may output a second reference shift clock to the second clock line as the second shift clock when the mode setting signal is at a first level, and may output the second reference shift clock to the first clock line as the first shift clock and may output the first reference shift clock to the second clock line as the second shift clock when the mode setting signal is at a second level.

According to this feature, the arrangement order of the gray-scale data and the capture start order of the gray-scale data necessary for a comb-tooth drive can be changed by setting the mode setting signal corresponding to the mounting state of the display driver.

This display driver may include a shift clock generation circuit which generates the first and second reference shift clocks based on a reference clock, and a shift operation period by each of the first and second shift registers may include a period in which phases of the first and second reference shift clocks are reversed.

With this display driver, the first and second shift start signals may be signals having the same phase, and the shift clock generation circuit may generate the second reference shift clock by dividing frequency of the reference clock and may generate the first reference shift clock which has a pulse in a first-stage capture period for capturing the first shift start signal into the first shift register and has a phase which is a reverse of a phase of the second reference shift clock in a data capture period after the first-stage capture period has elapsed.

According to these features, generation of the first and second reference shift clocks (first and second shift clocks) can be simplified, and the first and second shift start signals may be signals having the same phase. Therefore, the configuration and control of the display driver can be simplified.

With this display driver, a direction from the first side to the second side in which the data lines extend may be the same as the first or second shift direction.

With this display driver, when the scan lines extend along a long side of the electro-optical device and the data lines extend along a short side of the electro-optical device, the display driver may be disposed along the short side.

According to these features, the mounting size of the comb-tooth distributed electro-optical device can be reduced as the number of data lines increases.

Another embodiment of the present invention provides an electro-optical device including:

a plurality of scan lines;

a plurality of data lines which includes data line groups alternately distributed from two opposite sides toward inside of the electro-optical device in a shape of comb teeth, each of the data line groups consisting of a predetermined number of the data lines;

a switching element connected with one of the scan lines and one of the data lines; and

a pixel electrode connected with the switching element;

the above display driver which drives the data lines; and

a scan driver which scans the scan lines.

A further embodiment of the present invention provides an electro-optical device including:

a display panel which has first and second sides facing each other and includes a plurality of scan lines, a plurality of data lines which includes data line groups alternately distributed from the first and second sides toward inside of the electro-optical device in a shape of comb teeth, a switching element connected with one of the scan lines and one of the data lines, and a pixel electrode connected with the switching element, each of the data line groups consisting of a predetermined number of the data lines;

the above display driver which drives the data lines; and

a scan driver which scans the scan lines.

According to these embodiments, an electro-optical device which can be readily

mounted on an electronic instrument by reducing the mounting size can be provided.